REMARKS

Claims 1-22 are currently pending. Claims 1-22 are rejected. No new matter has been added.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-6, 10-15, 19-22 stand rejected under 35 USC 102(b) as being anticipated by U.S. Patent Number 5,933,356 to Rostoker et al., (Hereafter "Rostoker"). Applicants respectfully traverse this rejection on the basis of the following arguments.

Summary of Rostoker (5,933,356)

The Rostoker reference is directed to a system and method for creating and validating an electronic design structural description of a circuit or device from a VHDL description of the circuit or device. The system includes a compiler for compiling the VHDL description of the circuit or device, a device for locating problems within the compiled description and measuring the effectiveness of solving the problems, a device for passing information including the compiled description to a physical design level, a physical design tool for receiving the information and creating a physical design therefrom, and a device for back annotating the information from the physical design tool to the compiler.

Claim 1

Applicants maintain Rostoker fails to disclose each and every element of claim 1. The Examiner appears to be confusing a design tool of Rostoker with the analysis of a simulation output as set forth in claim 1. These are not the same thing. The teachings of the present invention are performed on the simulation of the design disclosed in Rostoker.

Rostoker is directed to a method and system for designing and modeling of electronic circuits or devices from a behavior description, namely VHDL, which can then be simulated and used in the physical design of the circuit or device. In other words Rostoker is only directed to the design and simulation of an electronic circuit or device. Rostoker does not disclose analyzing the information in the simulation output regarding the data signal and the clock signal and for producing a report of results of the analysis as set forth in claim 1. Rostoker deals with

designing and simulating an electronic circuit. The present invention deals with analysis after a simulation has been performed. This is not disclosed in Rostoker.

The citation Examiner has indicated as disclosing providing an automated tool for analyzing the information in the simulation output regarding the data signal and the clock signal and for producing a report of results of the analysis [Automated Design: Summary (Col. 29, line 50–Col. 30, line 17)] is actually directed to the design and modeling of electronic circuits or devices. Indeed, this section indicated by the Examiner is entitled "Automated Design: Summary." As indicated by the title it sets forth steps for creating a circuit design from a hardware description language such as VHDL. It does not disclose analyzing the information in the simulation output regarding the data signal and the clock signal and for producing a report of results of the analysis. Indeed there is no mention of simulation at all in this section cited by the Examiner. This section (Col. 29, line 50–Col. 30, line 17) is cited by the examiner as disclosing "providing an automated tool for analyzing the information in the simulation output regarding the data signal and the clock signal and for producing a report of the results of the analysis." While this section may disclose an automated tool, it is not for "analyzing the information in the simulation output." This section is a design tool. There is no mention of simulation in this section not analysis of the simulation output. As such, it does not disclose providing an automated tool for analyzing the information in the simulation output regarding the data signal and the clock signal and for producing a report of results of the analysis as set forth in claim1.

The only thing disclosed and taught in Rostoker is the design and simulation of a circuit. In contrast, the present invention performs analysis on simulation output such as provided by Rostoker. The citation the Examiner has indicated as disclosing performing the analysis of the simulation output with the tool to produce the report of the analysis actually reinforces the difference. The citation states: "The logic simulator takes the schematic object file and simulation models, *and generates a set of simulation results*" (Emphasis added). That is the "logic simulator" (not analyzer) takes the "schematic object file and simulation models" (the circuit design) and generates a set of "simulation results" (simulation output). There is no mention whatsoever of performing analysis on the simulation output as set forth in claim 1. The generation of simulation results is not the same thing as analysis of simulation results. As such,

Rostoker fails to disclose performing the analysis of the simulation output with the tool to produce the report of the analysis as set forth in claim1.

Thus, Rostoker fails to disclose each and every element of claim 1. Therefore, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claim 1 under 35 USC § 102.

Claims 2-6

Claims 2-6 depend from claim 1 and as such incorporate each and every element of claim 1. As discussed above Rostoker fails to disclose each and every element of claim 1. As such Rostoker fails to teach each and every element of claims 2-6.

Therefore, in view of the above arguments, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claims 2-6 under 35 USC § 102.

Claim 10

Rostoker fails to disclose each and every element of claim 10. As discuss above in regard to claim 1, Rostoker is directed to a method and system for designing and modeling of electronic circuits or devices from a behavior description, namely VHDL, which can then be simulated and used in the physical design of the circuit or device. In other words Rostoker is only directed to the design and simulation of an electronic circuit or device. In contrast claim 10 is directed to performing analysis on a simulation output, such as disclosed in Rostoker. As such there is no receiving of user-specified parameters which are applied to configure the analysis as set forth in claim 10. Thus, there is no performing the analysis of the simulation output with the tool to produce the report of the analysis as set forth in claim 10.

The citation the Examiner has indicated as disclosing receiving user-specified parameters and applying the user-specified parameters to configure the analysis performed [Column 22, lines 38-42] is actually directed to the optimization of the circuit design by the design compiler. It does not disclose the analysis. As such, Rostoker fails to disclose receiving user-specified parameters and applying the user-specified parameters to configure the analysis performed as set forth in claim 10.

As discussed above, the citation the Examiner has indicated as disclosing performing the analysis of the simulation output with the tool to produce the report of the analysis: "The logic simulator takes the schematic object file and simulation models, and generates a set of simulation results, acting on instructions initial conditions and input signal values provided to it either in the form of a file or user input" actually just indicates that a simulation output is generated. It does not disclose performing an analysis of the simulation output. As such, Rostoker fails to disclose performing the analysis of the simulation output with the tool to produce the report of the analysis as set forth in claim 10.

Thus, for the reasons as set forth above, Rostoker fails to disclose each and every element of claim 10. Therefore, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claim 10 under 35 USC § 102.

Claims 11-15

Claims 11-15 depend from claim 10 and as such incorporate each and every element of claim 10. As discussed above Rostoker fails to disclose each and every element of claim 10. As such Rostoker fails to teach each and every element of claims 11-15.

Therefore, in view of the above arguments, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claims 11-15 under 35 USC § 102.

Claims 19 and 22

Rostoker fails to disclose each and every element of claims 19 and 22. Specifically, Rostoker fails to disclose "with an automated analysis facility, processing the results of the simulation to identify data jitter for the data signal.

The citation Examiner has indicating as disclosing processing the results of the simulation to identify data jitter for the data signal [Timing constraints may include the following: maximum and minimum rise/fall delay, set-up and hold check, length of clock cycle and maximum transition time per net. The timing constraints may also include boundary conditions, such as signal skew and the module's inputs, drive capabilities of the modules

outputs, etc., when such data is available (Col. 20, lines 31-37)] is actually directed to the behavior description of modeled circuit or device for the purposes of design and simulation. That is the timing constraints define how a circuit or device behaves so that is can be simulated. It does not disclose processing the results of the simulation to identify jitter as set forth in claims 19 and 22.

Thus, Rostoker fails to disclose each and every element of claims 19 and 22. Therefore, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claims 19 and 22 under 35 USC § 102.

Claims 20 and 21

Claims 20 and 21 depend from claim 19 and as such incorporate each and every element of claim 19. As discussed above Rostoker fails to disclose each and every element of claim 19. As such Rostoker fails to teach each and every element of claims 20 and 21.

Therefore, in view of the above arguments, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claims 20 and 21 under 35 USC § 102.

Claim Rejections under 35 USC § 103

Claims 7, 8, 16, and 17 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker in view of Nourani, Mehradad et al., "Built-In Self-Test for signal Integrity" June 18, 2001 pages 792-797, (Hereafter "Nourani'). Claims 9 and 18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker in view of "Inside differential signals" by Cadence, 2001, retrieved from winnet.com.cn/Cadence/High_Speed_Design/ Inside_Differential_Signals.pdf, (Hereafter "Cadence"). Applicants respectfully traverse the rejections in view of the following arguments.

Claims 7, 8, 16, and 17

Claim 7, 8, 16, and 17 depend from claims 1 and 10 and as such incorporates each and every element of claims 1 and 10. As discussed above with regard to the 35 USC 102 rejection, Rostoker is directed to design and modeling of electronic circuits and devices. Claims 1 and 10

are directed to analysis of a simulation output. The elements of claims 1 and 10 the Examiner has indicated as being directed to the analysis elements of clams 1 and 10 are actually directed the aspects of the design process. Designing a circuit and analyzing a simulation output are separate and distinct concepts. Therefore, Applicants respectfully submit that Rostoker neither teaches nor suggests each and every element of claims 1 and 10. As such, Rostoker fails to teach or suggest each and every element of claims 7, 8, 16, and 17. The combination of Nourani with Rostoker as suggested by the Examiner fails to cure this deficiency.

In light of the above comments, applicants respectfully submit that each and every element of claims 7, 8, 16, and 17 of the present invention are not taught or suggested by either Rostoker or Nourani, and therefore claims 7, 8, 16, and 17 are in condition for allowance over Rostoker or Nourani.

Therefore, in view of the above arguments, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claims 7, 8, 16, and 17 under 35 USC § 103.

Claims 9 and 18

Claim 9 and 18 depend from claims 1 and 10 and as such incorporates each and every element of claims 1 and 10. For the reasons discussed above, Applicants respectfully submit that Rostoker neither teaches nor suggests each and every element of claims 1 and 10. As such, Rostoker fails to teach or suggest each and every element of claims 9 and 18. The combination of Cadence with Rostoker as suggested by the Examiner fails to cure this deficiency.

In light of the above comments, applicants respectfully submit that each and every element of claims 9 and 18 of the present invention are not taught or suggested by either Rostoker or Cadence, and therefore claims 9 and 18 are in condition for allowance over Rostoker or Cadence.

Therefore, in view of the above arguments, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claims 9 and 18 under 35 USC § 103.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this statement. However, if a fee is due, please charge our Deposit Account No. 12-0080, under Order No. SMQ-044 from which the undersigned is authorized to draw.

Dated: March 13, 2005

Respectfully submitted,

By _____

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